ABSTRACT OF THE DISCLOSURE

A latch circuit includes a sample section for responding to complementary clock signals to sample complementary data signals during a sample period, a latch section for latching the sampled complementary data signals on latch output nodes to transfer the same through latch output nodes during a hold period, and a precharge section for precharging the latch output nodes during the sample period. The latch circuit has a smaller dead zone including a smaller setup time and a smaller hold time.